UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,853	10/28/2003	Krishna K. Pappu	03-0128 81615	6739

7590 04/24/2006

Leo J. Peters
LSI Logic Corporation
MS D-106
1551 McCarthy Blvd.
Milpitas, CA 95035

EXAMINER	
PARIHAR, SUCHIN	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 04/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/695,853	PAPPU ET AL.	
	Examiner	Art Unit	
	Suchin Parihar	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/695,853, amendment filed on 2/15/2006. Claims 1-3, 5-12 and 14-18 are currently amended. Claims 1-18 are pending in this application.

2. Applicant's arguments filed 1/26/2006 have been fully considered but they are not persuasive. The applicable rejections from the prior office action are incorporated herein.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 1-3, 5-12, and 14-18 are rejected under 35 U.S.C. 103(a)** as being unpatentable over Huang et al. (US 2004/0015803) in view of Nadeau-Dostie et al. (6,457,161).

5. With respect to claims 1 and 10, Huang et al. teaches a method of grouping cells of an integrated circuit, which includes teaching a computer program/computer program product (pg 1, paragraph [0005], i.e. CAD tool), comprising the steps of: (a) receiving as input a representation of an integrated circuit design (Fig 6, 602, i.e. HDL Description); (b) initializing a corresponding list of cells for a common signal domain in the integrated circuit design (pg 3, paragraph [0024], i.e. netlist received from design database, cells triggered by one or more source clocks – "common signal domain"); (c) selecting a cell

belonging to a common signal domain (i.e. same source clock) that is not included in a corresponding list of cells (i.e. subgroups) for a common signal domain (pg 3, paragraph [0024], i.e. scan cells partitioned into subgroups based upon source clocks); and (e) and (g) inserting (i.e. partitioning into subgroups which effectively results in inserting the selected cells) the selected cell in the corresponding list of cells (i.e. subgroups) for the common signal domain (i.e. same clock source) associated with the signal driver. Huang et al. does not specifically teach tracing steps that involve: (d) tracing a net from an input port of the selected cell to a signal driver; and (f) tracing the net to an input port of each cell connected to the signal driver. Nadeau-Dostie et al. teaches a method/computer-tool for representing a circuit that involves: (d) tracing a net from an input port of the selected cell to a signal driver (i.e. tracing backward from the clock input of the latch to a clock source, Col 8, lines 10-12); and (f) tracing the net to an input port of each cell connected to the signal driver (the output of the multiplexer [i.e. signal-driving element] is connected [i.e. effectively traced] to the data input of the D-latch, Col 6, lines 20-22). It would have been obvious to one with ordinary skill in the art at the time of the invention to incorporate the teachings of Nadeau-Dostie et al. into the method/program of Huang because the tracing step as taught by Nadeau-Dostie et al. would provide for the necessary identification of the scan cells for selection and further insertion into the lists (i.e. for proper partitioning of scan cells into subgroups) that correspond to a particular source clock root (i.e. common signal domain) of the method/system of Huang.

6. With respect to claims 2 and 11, Huang et al. in view of Nadeau-Dostie et al. teaches all the elements of claims 1 and 10, from which the respective claims depend, as described above. Huang also teaches repeating steps (c), (d), (e), (f) and (g) until every cell belonging to a common signal domain has been inserted in a corresponding list of cells for the common signal domain, (the scan cells are partitioned into subgroups based upon source clock roots, pg 3, paragraph [0024]) (i.e. repetition of steps must occur in order to place all cells into their corresponding lists/subgroups) wherein it is within the scope of Huang et al. that the steps (c), (d), (e), (f) and (g) must be repeated in order to partition all cells into a particular subgroup (i.e. insert each cell into a list of cells).

7. With respect to claims 3 and 12, Huang et al. in view of Nadeau-Dostie et al. teaches all the elements of claims 2 and 11 respectively, from which the respective claims depend, as described above. Huang et al. also teaches generating as output a corresponding list of cells (pg 6, paragraph [0060], i.e. a net-list is output) for a common signal domain (i.e. same source clock) in the integrated circuit design. Note that said net-list of Huang may contain groups of scan-chains wherein the cells of these chains have been grouped by having a common source clock.

8. With respect to claims 5 and 14, Huang et al. in view of Nadeau-Dostie et al. teaches all the elements of claims 1 and 10, from which the respective claims depend, as discussed above. Huang et al. also teaches performing steps (b), (c), (d), (e), (f) and (g) for cells that are flip-flops in a scan chain (pg 1, paragraph [0007], i.e. sequential cells, D-flip-flops, SR, JK).

9. With respect to claims 6 and 15, Huang et al. in view of Nadeau-Dostie et al. teaches all the elements of claims 5 and 14, from which the respective claims depend, as discussed above. Huang also teaches performing steps (b), (c), (d), (e), (f) and (g) for a common signal domain that is a scan clock domain (pg 3, paragraph [0024], i.e. scan cells having same source clock root).

10. With respect to claims 7 and 16, Huang et al. in view of Nadeau-Dostie et al. teaches all the elements of claims 6 and 15, from which the respective claims depend, as discussed above. Huang et al. also teaches performing steps (d), (e), (f) and (g) for a net that is a clock net (pg 3, paragraph [0024], i.e. grouping cells based on clock tree roots).

11. With respect to claims 8 and 17, Huang et al. in view of Nadeau-Dostie et al. teaches all the elements of claims 7 and 16 respectively, from which the claims depend. Haung et al. in view of Nadeau-Dostie et al. also teaches performing steps (d), (e), (f) and (g) for an input port that is a clock port because the tracing steps (d), (e), (f) and (g) of Nadeau-Dostie et al. also applies for an input port that is a clock port (Col 8, lines 10-11, i.e. tracing backward to determine clock path), and Huang et al. discusses the connection relationship between a clock input port (pg 3, paragraph [0024], i.e. scan cell trigger) and a signal driver (i.e. clock source), that needed to be traced in order to arrive at the proper scan cell partitioning.

12. With respect to claims 9 and 18, Huang in view of Nadeau-Dostie teaches all the elements of claims 8 and 17, from which the respective claims depend, as discussed above. Huang et al. in view of Nadeau-Dostie et al. also teaches performing steps (d),

(e), (f) and (g) for a signal driver that is a clock driver because the tracing steps (d), (e), (f) and (g) of Nadeau-Dostie et al. also applies for a signal driver that is a clock driver (Col 8, lines 10-11, i.e. clock source driver) and Huang et al. also discusses the connection relationship between a clock input port (pg 3, paragraph [0024], i.e. scan cell trigger) and a clock driver (i.e. clock source) that needed to be traced in order to arrive at the proper scan cell partitioning.

13. **Claims 4 and 13 are rejected under 35 U.S.C. 103(a)** as being unpatentable over Huang et al. (US 2004/0015803) in view of Nadeau-Dostie et al. (6,457,161) and further in view of Yoshimoto (6,877,120).

14. With respect to claims 4 and 13, Huang et al. in view of Nadeau-Dostie et al. teaches all the elements of claim 1 and 10, from which the claims depend respectively, as discussed previously. Huang et al. in view of Nadeau-Dostie et al. does not teach a list of cells for a common signal domain in which the names of the cells are stored. However, Yoshimoto teaches a method wherein a file contains a list of scan chains that contain the names of the scan elements stored in a particular order of the chain so that the scan cells can be quickly and reliably searched (Col 1, lines 21-64). It would have been obvious to incorporate Yoshimoto into the method/program of Huang et al. in view of Nadeau-Dostie et al. because the scan chain information that is generated in Yoshimoto (Col 1, lines 55-60, i.e. including names of cells) makes the method/program of Huang et al. in view of Nadeau-Dostie et al. faster by providing a searchable information-file that can be quickly and reliably accessed to retrieve information such as the names associated with each cell in a circuit.

Response to Arguments

15. Applicant's arguments filed 1/26/2006 have been fully considered but they are not persuasive.

16 Applicant argues that Huang et al. lacks the claimed steps (c) and (e). Specifically, Applicant argues that Huang does not teach: (c) selecting a cell belonging to a common signal domain that is not included in a corresponding list of cells for a common signal domain; and (e) inserting the selected cell in the corresponding list of cells for the common signal domain associated with the signal driver. Examiner disagrees with this assertion.

17. In order to insert a selected cell into a corresponding list (i.e. Huang's groups/subgroups) as claimed in step (e), a cell belonging to a common signal domain (Huang's source clock root) must first be selected. In other words, the existence of a step (e) necessarily requires that a step (c) be performed apriori, irrespective of whether is it explicitly stated. Although Huang does not explicitly recite a step of selecting a cell (step c), Huang does disclose the step of inserting a cell. Examiner asserts that step (c) is implicit in the method of Huang, and is sufficient to support a rejection under 35 U.S.C. 103(a).

18. Applicant argues that one of ordinary skill in the art would not be motivated, at the time of the invention, to modify Huang by the tracing module of Nadeau to identify scan cells for selection and insertion into lists. Examiner respectfully disagrees with this assertion. The claimed invention inserts selected cells into corresponding lists. The prior art of Huang teaches partitioning cells into subgroups. The partitioning of cells in

Huang constitutes the selected cells being inserted into the corresponding lists of cells; and the subgroups of Huang correspond with the list of cells.

19. Contrary with the applicant's assertion, the claimed lists are not necessary to achieve the partitioning. Rather, the claimed lists are a result of the partitioning.

20. With respect to the motivation to combine, Examiner responds as follows: Huang teaches the partitioning of scan cells into subgroups based upon source clock roots (i.e. inserting cells into corresponding lists). Huang does not teach a method of determining the source clock root (i.e. common signal domain) of a particular scan cell. Nadeau-Dostie teaches a method for determining a source clock root (i.e. common signal domain) of a particular cell by tracing backward from the clock input of a latch (i.e. input port of a cell) to a clock source (i.e. signal driver, signal domain). Moreover, in order for the claimed invention to determine the signal domain (i.e. source clock root) of a particular selected cell, a step such as the tracing step (d) or (f) must be performed to determine which of the claimed lists is the appropriate corresponding list to which the cell should be inserted. This determining step is provided by Nadeau-Dostie. Therefore, sufficient motivation exists to modify Huang by the tracing module of Nadeau-Dostie.

21. In summary, Applicant fails to place claims 1-18 in condition for allowance. Examiner therefore maintains the rejections of claims 1-18 under 35 U.S.C. 103(a).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suchin Parihar whose telephone number is 571-272-6210. The examiner can normally be reached on Mon-Fri, 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Suchin Parihar
Examiner
AU 2825

A. M. Thompson
Primary Examiner
Technology Center 2800